

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
  - a plurality of memory blocks each including a plurality of memory cells arranged in rows and columns, a plurality of word lines respectively arranged correspondingly to a plurality of rows of said plurality of memory cells, and a plurality of pairs of bit lines respectively arranged  
5 correspondingly to a plurality of columns of said plurality of memory cells;
    - a plurality of sense amplifier bands provided correspondingly to each of said plurality of memory blocks to sense and amplify data read from said memory cells;
  - 10 a plurality of pairs of read data lines extended commonly from said plurality of sense amplifier bands; and
    - a logic circuit having input terminals connected to one pair of read data lines respectively of said plurality of pairs of read data lines,
      - 15 said logic circuit providing a self-precharge signal when an increased potential difference is generated between the pair of read data lines connected respectively to the input terminals.
2. The semiconductor memory device according to claim 1, wherein said plurality of sense amplifier bands each include a read gate circuit provided correspondingly to each of said plurality of pairs of bit lines for reading data onto said pair of read data lines,
  - 5 said read gate circuit including
    - a first transistor having its gate connected to one of said paired bit lines and its source dynamically changing according to activation/inactivation of said sense amplifier band, and
    - 10 a second transistor having its gate connected to the other of said paired bit lines and its source dynamically changing according to activation/inactivation of said sense amplifier band.
3. The semiconductor memory device according to claim 1, further comprising a central control circuit providing an internal precharge signal

when receiving said self-precharge signal or an external precharge signal.

4. The semiconductor memory device according to claim 1, wherein said pair of read data lines connected respectively to the input terminals of said logic circuit is a pair of read data lines except for a pair of read data lines having the longest distance from one of said plurality of sense amplifier bands to the input terminals of said logic circuit.

5 5. The semiconductor memory device according to claim 4, wherein said pair of read data lines connected respectively to the input terminals of said logic circuit has the shortest distance from one of said plurality of sense amplifier bands to the input terminals of said logic circuit.

6. The semiconductor memory device according to claim 1, further comprising an input/output selection circuit selecting one pair of read data lines from said plurality of pairs of read data lines to connect the selected pair of read data lines respectively to the input terminals of said logic circuit.

7. The semiconductor memory device according to claim 1, wherein onto said pair of read data lines connected respectively to the input terminals of said logic circuit, among said plurality of pairs of read data lines, read data is allowed to be read in read operation and write operation and, onto any pair of read data lines except for said pair of read data lines connected respectively to the input terminals of said logic circuit, read data is allowed to be read in read operation only.

8. The semiconductor memory device according to claim 1, wherein said logic circuit is an XOR circuit.

9. The semiconductor memory device according to claim 1, wherein said logic circuit is a NAND circuit.